Amendments to the Specification

Please replace the paragraph beginning on page 13, line 9, with the following amended paragraph:

Fig. 2B is a circuit diagram of an example of the boost circuit 138, the sub-array decoder 262, the word line driver 208, the single word line leak-current limited units 124 and the sub-array word line leak-current limited unit 126. In normal mode, PRECH 232 is at high state; LKSPN 234 is at high state; and BOOST 134 is at low state. The MOS transistor 236 is used to precharge the node VH 240 to the power level of VCC 238~~, the highest voltage during normal mode,~~ before issuing a RAS command. When a RAS command is issued, PRECH 232 is at low state; LKSPN 234 is at low state; and BOOST 134 is at high state. The charge stored on the capacitor C 242 is dumped to the node VH 240 and the PMOS transistor 244 is used to sustain the leakage current of an active word line for a long RAS cycle operation.

Please replace the paragraph beginning on page 22 line 1, with the following amended paragraph:

When the first input voltage 412 is lower than the reference input voltage 422, the first output voltage signal 418 is pulled high to turn on the MOS transistor 426 and to supply current from the high ~~reference~~ voltage source 423 to the cell plate voltage, VEQ 136. When the second input voltage 414 is higher than the reference input voltage 422, the second output voltage signal 420 is pulled high to turn on the MOS transistor 428 and the current is sunk from the cell plate voltage, VEQ 136, to the low voltage source 424. The voltage generator 400 doesn't supply or sink current for the cell plate voltage, VEQ 136, in a well-defined range. The range is given by

~~VCC-(VCC-Vref)*(R1+R2+R3)/R1 < VEQ < VCC-(VCC-Vref)*(R1+R2+R3)/(R1+R2)~~

VCC-(VCC-Vref)*(R1+R1+R3)/R1 < VEQ < VCC-(VCC-Vref)*R1+R2+R3)/(R1+R2)

where VCC is, for example, the high reference voltage 416; Vref is the reference input voltage 422; and R1 456, R2 458, and R3 460 are the resistors in the voltage dividing circuit 402.

Please replace the paragraph beginning on page 23 line 11, with the following amended paragraph:

The data-in setup time, Tds 502, and the data-in hold time, Tdh 504, is reserved at the rising edge [[506]] 507 and the falling edge 508 of the alternately switching cell plate voltage, VEQ 136. By alternately switching ODD 146 and EVEN 148, as shown in Fig. 5, the even word lines and the odd word lines are grouped by EVEN 148 and ODD 146, respectively, and the word line stress voltage is applied to the even word lines and to the odd word lines alternately. In Fig. 2B, the even word lines are represented by WL_(2n) 211 and the odd word lines are represented by WL_(2n-1) 215. The time needed for the word line transition delay, Td 506, is placed between the alternately switching word line stress voltage applied to the even word lines 211 and the odd word lines 215.

Amendments to the Drawings

Applicants amend the drawings as specified below. Annotated drawing sheets are attached hereto at Exhibit A, and clean (revised) drawing sheets are attached hereto at Exhibit B.

Fig. 1C is amended by reversing (horizontally) the direction of the input buffer 182.

FIG. 2B is amended to change NOR three gates to NAND gates.

FIG. 3B is amended to delete a connection point (near reference numeral 340).

FIG. 4B is amended to change reference numeral "125" to "128".

FIG. 5 is amended to change reference numeral "506" to "507".

Attachments:

Exhibit A: Annotated version of amended drawing sheets.

Exhibit B: Clean/revised version of amended drawing sheets.